



1748

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Charles W.C. Lin

Title: SUPPORT CIRCUIT WITH A TAPERED THROUGH-HOLE
FOR A SEMICONDUCTOR CHIP ASSEMBLY

Serial No.: 10/002,732 Filed: November 15, 2001

Examiner: Unknown Group Art Unit: Unknown

Atty. Docket No.: P012-1

#5/IDS
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ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

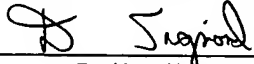
Pursuant to Applicant's duty of disclosure under 37 C.F.R. § 1.56 and §§ 1.97-1.98, Applicant hereby provides a copy of the documents identified on the enclosed Form PTO-1449.

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, an admission that any of these documents, alone or in any combination, is considered to be material to patentability, an admission that any of these documents is prior art as to the above-identified application, or an admission against interest in any manner.

This Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits. Accordingly, no fee is due. 37 C.F.R. § 1.97(b)(3).

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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on December 17, 2001.



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12/17/01

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Respectfully submitted,



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Form PTO-1449

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10/002,732

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Applicant

Charles W.C. Lin

Filing Date

November 15, 2001

Group Art Unit

U.S. Patent Documents

*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
AA						

Foreign Patent Documents

							Translation	
	Document	Date	Country	Class	Subclass		Yes	No
AB								

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

AC	U.S. Application Serial No. 09/120,408, filed July 22, 1998, entitled "Flip Chip Assembly With Via Interconnection"
AD	U.S. Application Serial No. 09/643,212, filed August 22, 2000, entitled "Semiconductor Chip Assembly With Simultaneously Electroplated Contact Terminal and Connection Joint"
AE	U.S. Application Serial No. 09/643,214, filed August 22, 2000, entitled "Semiconductor Chip Assembly with Simultaneously Electrolessly Plated Contact Terminal and Connection Joint"
AF	U.S. Application Serial No. 09/643,213, filed August 22, 2000, entitled "Method Of Making A Support Circuit For A Semiconductor Chip Assembly"
AG	U.S. Application Serial No. 09/643,445, filed August 22, 2000, entitled "Method Of Making A Semiconductor Chip Assembly"
AH	U.S. Application Serial No. 09/665,928, filed September 20, 2000, entitled "Semiconductor Chip Assembly With Ball Bond Connection Joint"

Examiner

Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your next communication to Applicant.

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